	Application No.	Applicant(s)
Notice of Allowability	10/088,106	NAKATSUJI ET AL.
	Examiner	Art Unit
	Sherrie Hsia	2614
	Sherrie Hsia	2014
The MAILING DATE of this communication appears on the cover sheet with the correspondence addressAll claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308. 1. This communication is responsive to the IDS filed on 8/8/05. 2. The allowed claim(s) is/are claims 1-7, 9, 11, 14, 10, 12, 15, 8, 13, 16-23, 25, 27, 26, 28, 24, and 29-31 (renumbered as claims 1-31 respectively).		
3. The drawings filed on 22 March 2002 are accepted by the Examiner.		
4.		
 Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/08 Paper No./Mail Date 8/8/05 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. ☐ Interview Summary (Paper No./Mail Date 8), 7. ☐ Examiner's Amendm	ė

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1. The following is an examiner's statement of reasons for allowance: the prior art (U.S. Patent No. 5764297 and JP 10-042163, cited by applicant) fail to show or fairly suggest an image distortion correcting method and apparatus for correcting distortion in an image displayed on a screen on the basis of a video signal having the combinations as claimed, including a storage device, a write clock signal generation circuit, a read clock signal generation circuit, a distortion correction waveform generation circuit for generating a distortion correction waveform for correcting the distortion in the image by shifting the positions of pixels displayed on the screen on the basis of the video signal and a read clock signal control circuit for controlling the frequency of the read clock signal generated by the read clock signal generation circuit on the basis of the distortion correction waveform generated by the distortion correction waveform generation circuit setting the distortion correction waveform such that the amount of shift of the pixel reaches zero at both ends and the center of the image in the horizontal scanning direction, as recited in the claims.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sherrie Hsia whose telephone number is (571) 272-7347.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Or faxed to:

(571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office whose telephone number is (703) 308-HELP.

Sherrie Hsia
Primary Examiner
Art Unit 2614

SH August 19, 2005